CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Currently Amended) A differential transistor pair~~, comprising a plurality of transistor cells in a substrate, each~~ **comprising a first and second transistor, said first and second transistors comprising at least one transistor cell provided in a substrate, the at least one** cell comprising:

~~- first drain/collector regions at the respective edge of the cell~~ **a first and a second drain/collector region belonging to the first transistor of said differential transistor pair and arranged separated from each other**,

~~- a second drain/collector region between the first drain/collector regions~~ **a third drain/collector region belonging to the second transistor of said differential transistor pair, and arranged between said first and second drain/collector regions**,

- **a first** source/emitter ~~regions between the respective~~ **region arranged between said** first drain/collector region and ~~the second~~ **said third** drain/collector region, **and a second source/emitter region arranged between said second drain/collector region and said third drain/collector region, said source/emitter regions being common to both transistors of the differential transistor pair,**

- a first and a second gate/base region belonging to the first transistor of said differential transistor pair, said first gate/base region being arranged between said first drain collector region and the first source/emitter region, and said second gate/base region being arranged between said second drain/collector region and the second source/emitter region ~~first gate/base regions between the respective first drain/collector region and the source/emitter regions~~, and

- a third and a fourth gate/base region belonging to the second transistor of said differential transistor pair, said third gate/base region being arranged between said

third drain/collector region and the first course/emitter region, and said fourth gate/base region being arranged between said third drain/collector region and the second source/emitter region.

~~**second gate/base regions between the source/emitter regions and the second drain/collector region, wherein**~~

~~**the first drain/collector regions of all cells being interconnected to a common first drain/collector terminal,**~~

~~**the second drain/collector region of all cells being interconnected to a common second drain/collector terminal,**~~

~~**the first gate/base regions of all cells being interconnected to a common first gate/base terminal, and**~~

~~**the second gate/base regions of all cells being interconnected to a common second gate/base terminal.**~~

2. (Cancelled)

3. (Cancelled)

4. (New) The differential transistor pair as claimed in claim 1, comprising a plurality of transistor cells, wherein

- the first and second drain/collector regions of each of said plurality of transistor cells of said first transistor are interconnected to a common first drain/collector terminal,

- the third drain/collector region of each of said plurality of transistor cells of said second transistor are interconnected to a common second drain/collector terminal,

- the first and second gate/base regions of each of said plurality of transistor cells of said first transistor are interconnected to a common first gate/base terminal, and

- the third and fourth gate/base regions of each of said plurality of transistor cells of said second transistor are interconnected to a common second gate/base terminal.

5. (New) The differential transistor pair as claimed in claim 1, for use in RF power amplifier applications.

6. (New) The differential transistor pair as claimed in claim 1, wherein said differential transistor pair is a differential LDMOS transistor pair or a differential bipolar junction transistor pair.

7. (New) The differential transistor pair as claimed in claim 1, wherein each of said first and second transistors has a finger type layout.